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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,917	12/16/2003	Yoshihiro Koga	60188-732	3835

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EXAMINER	
VO, THANH DUC	

ART UNIT	PAPER NUMBER
2189	

MAIL DATE	DELIVERY MODE
09/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/735,917	KOGA ET AL.	
	Examiner	Art Unit	
	Thanh D. Vo	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,17,18,20,21,23,24,26,27,29-31,33,34,36,37,39,40 and 42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,17 and 30* is/are rejected.

7)☒ Claim(s) *18,20,21,23,24,26,27,29,31,33,34,36,37,39,40 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is responsive to the Amendment filed on 11/01/2007. Claims 1-3, 17, 18, 20, 21, 23, 24, 26, 27, 29-31, 33, 34, 36, 37, 39, 40, and 42 are presented for examination. Claims 1-3, 17, 18, 20, 21, 23, 24, 26, 27, 29-31, 33, 34, 36, 37, 39, 40, and 42 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. (US Patent 5,361,340) in view of Tran (US Patent 5,900,012).

As per claim 1, Kelly et al. discloses a semiconductor device comprising:

a processor (Fig. 2, item 12);

a first memory unit accessed by the processor and serving as a main memory (Fig. 2, item 22);

a plurality of page memory units obtained by partitioning a second memory unit (col. 5, lines 59-60, virtual cache) which is different from the first memory unit and accessible within several clock cycles by the processor at a speed higher than a speed at which the first memory unit is accessible and serves as a cache memory such that

each of the page memory units has a storage capacity of several kilobytes (See col. 5, lines 59-66);

Kelly et al. does not particularly disclose a tag for adding, to each of the page memory units, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority;

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag; and

a replacement control unit for replacing respective contents of the page memory units.

Tran discloses a tag for adding, to each cache line, tag information indicative of an address value in the first memory unit and priority information indicative of a replacement priority (See col. 7, lines 36-51);

a tag comparator for comparing, upon receipt of an access request from the processor, the address value in the first memory unit with the tag information held by the tag (See col. 7, lines 36-38); and

a replacement control unit for replacing respective contents of the cache line (See col. 7, lines 43-45).

It would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to modify the invention of Kelly et al. to include method taught by Tran in order to arrive at the current invention. The motivation of doing so is allow the system of Kelly et al. to coordinately checking for the most recently used content in

a page memory unit and to be replaced by the most recently used content since it is known to one having an ordinary skill in the art that the most recently used content are more likely to be accessed. Such replacement method improve the system performance because the data need to be used is readily provided at the cache level.

3. Claims 2, 3, 17, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelly et al. (US Patent 5,361,340) in view of Tran (US Patent 5,900,012) and further in view of Yamazaki (US Patent 6,233,195).

As per claim 2, Kelly et al. does not particularly disclose the semiconductor device of claim 1, further comprising:

a distribution managing unit for managing a number of pages allocated to each of the page memory units for each function of an application program executed by the processor.

Yamazaki et al. discloses a semiconductor device comprising:

a distribution managing unit for managing the number of pages allocated to each of the page memory units for each function of an application program executed by the processor. See col. 7, lines 35-44, wherein a plurality of pages are allocated or distributed to teach memory block (page memory unit). In addition, each function of an application program executed by the processor is an inherent feature in the device Yamazaki et al. since all command and/or instructions that are processed by the processor has to be executed using each of the memory block in the cache memory.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant invention to combine the method of Kelly et al. with the method of Yamazaki et al. in order to arrive at the current invention. The motivation of doing so is to improve the page hit rate as disclosed by Yamazaki et al. at col. 8, lines 59-61.

As per claim 3, Yamazaki et al. discloses a semiconductor, wherein the plurality of page memory units are assigned to groups each composed of a specified number of page memory units to compose a plurality of bank memories (col. 8, lines 7-13), the semiconductor device further comprising:

a bank control unit for managing the plurality of bank memories is an inherent feature since the device has to have a control unit to assign a plurality of page memory into each of the bank memory.

Therefore, it would have been obvious to one having an ordinary skill in the art at the time of the Applicant's invention to combine the method of Kelly et al. with the method of Yamazaki et al. in order to arrive at the current invention. The motivation of doing so is to improve the page hit rate as disclosed by Yamazaki et al. at col. 9, lines 5-8.

As to claims 17 and 30, Evans et al. discloses a replacement control unit determines whether or not information on a requested address is held in the tag upon receipt of an access request; select one of the plurality of page memory units if the

address information is not held in the tag based on preliminarily specified replacement information; transfers data of the requested address from the first memory unit into the page memory unit. See request and replacement procedure at col. 2, lines 29-42.

Allowable Subject Matter

4. Claims 18, 21, 24, 27, 31, 34, 37, and 40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 20, 23, 26, 29, 33, 36, 39, and 42 are also allowable since they are depending from allowable claims 18, 21, 24, 27, 31, 34, 37, and 40.

Response to Arguments

Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection necessitated by Applicant's Amendment.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh D. Vo whose telephone number is (571) 272-0708. The examiner can normally be reached on M-F 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thanh D Vo/

Examiner, Art Unit 2189

/Reginald G. Bragdon/
Supervisory Patent Examiner, Art Unit 2189